

Sub A1 1. A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing a first organic dielectric layer overlying said insulating layer;

depositing a second inorganic dielectric layer overlying said first dielectric layer;

etching a via pattern into said second dielectric layer;

etching said via pattern into said first dielectric layer using patterned said second dielectric layer as a mask; and

thereafter etching a trench pattern into said second inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

2. The method according to Claim 1 further comprising forming semiconductor device structures including gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact said semiconductor device structures.

Sub A2 3. The method according to Claim 1 wherein said first organic dielectric layer comprises one of the group containing: polyimides, HOSP, SILK, FLARE, BCB, MSQ, and organic polymers.

4. The method according to Claim 1 wherein said second inorganic dielectric layer comprises one of the group containing: CORAL, BLACK DIAMOND, FSG, carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, and HSQ.

5. The method according to Claim 1 further comprising filling said dual damascene openings with a metal layer.

Sub A3 6. A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:  
providing metal lines covered by an insulating layer overlying a semiconductor substrate;  
depositing a first organic dielectric layer overlying said insulating layer;  
depositing a second inorganic dielectric layer overlying said first dielectric layer;  
etching a trench pattern into said second dielectric layer; and  
thereafter etching a via pattern through said second inorganic dielectric layer and said first organic

dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

7. The method according to Claim 6 further comprising forming semiconductor device structures including gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact said semiconductor device structures.

Sub A4 8. The method according to Claim 6 wherein said first organic dielectric layer comprises one of the group containing: polyimides, HOSP, SILK, FLARE, BCB, MSQ, and organic polymers.

9. The method according to Claim 6 wherein said second inorganic dielectric layer comprises one of the group containing: CORAL, BLACK DIAMOND, FSG, carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, and HSQ.

10. The method according to Claim 6 further comprising filling said dual damascene openings with a metal layer.

Sub A5 11. A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing a first organic dielectric layer overlying said insulating layer;

depositing a second inorganic dielectric layer overlying said first dielectric layer;

etching a via pattern into said second dielectric layer; and

simultaneously etching said via pattern into said first dielectric layer and etching a trench pattern into said second inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

12. The method according to Claim 11 further comprising forming semiconductor device structures including gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact said semiconductor device structures.

*Sub 11*  
13. The method according to Claim 11 wherein said first organic dielectric layer comprises one of the group containing: polyimides, HOSP, SILK, FLARE, BCB, MSQ, and organic polymers.

14. The method according to Claim 11 wherein said second inorganic dielectric layer comprises one of the group containing: CORAL, BLACK DIAMOND, FSG, carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, and HSQ.

15. The method according to Claim 11 further comprising filling said dual damascene openings with a metal layer.

*Sub* 16. A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

- providing metal lines covered by an insulating layer overlying a semiconductor substrate;
- depositing a first inorganic dielectric layer overlying said insulating layer;
- depositing a second organic dielectric layer overlying said first dielectric layer;
- etching a via pattern into said second dielectric layer;
- etching said via pattern into said first dielectric layer using patterned said second dielectric layer as a mask; and
- thereafter etching a trench pattern into said second inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

17. The method according to Claim 16 further comprising forming semiconductor device structures including gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlies and contact said semiconductor device structures.

Sub AG 18. The method according to Claim 16 wherein said first inorganic dielectric layer comprises one of the group containing: CORAL, BLACK DIAMOND, FSG, carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, and HSQ.

19. The method according to Claim 16 wherein said second organic dielectric layer comprises one of the group containing: polyimides, HOSP, SILK, FLARE, BCB, MSQ, and organic polymers.

20. The method according to Claim 16 further comprising filling said dual damascene openings with a metal layer.

Sub AG 21. A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:  
providing metal lines covered by an insulating layer overlying a semiconductor substrate;  
depositing a first inorganic dielectric layer overlying said insulating layer;

depositing a second organic dielectric layer  
overlying said first dielectric layer;

etching a trench pattern into said second  
dielectric layer; and

thereafter etching a via pattern through said  
second inorganic dielectric layer and said first organic  
dielectric layer to complete said forming of said dual  
damascene openings in the fabrication of said integrated  
circuit device.

22. The method according to Claim 21 further comprising  
forming semiconductor device structures including gate  
electrodes and source and drain regions in and on said  
semiconductor substrate wherein said metal lines overlie  
and contact said semiconductor device structures.

*Sub A10* 23. The method according to Claim 21 wherein said first  
inorganic dielectric layer comprises one of the group  
containing: CORAL, BLACK DIAMOND, FSG, carbon-doped FSG,  
nitrogen-doped FSG, Z3MS, XLK, and HSQ.

24. The method according to Claim 21 wherein said second  
organic dielectric layer comprises one of the group  
containing: polyimides, HOSP, SILK, FLARE, BCB, MSQ, and  
organic polymers.

25. The method according to Claim 21 further comprising filling said dual damascene openings with a metal layer.

*Sub A11* 26. A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

- providing metal lines covered by an insulating layer overlying a semiconductor substrate;
- depositing a first inorganic dielectric layer overlying said insulating layer;
- depositing a second organic dielectric layer overlying said first dielectric layer;
- etching a via pattern into said second dielectric layer; and
- simultaneously etching said via pattern into said first dielectric layer and etching a trench pattern into said second inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

27. The method according to Claim 26 further comprising forming semiconductor device structures including gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact said semiconductor device structures.



28. The method according to Claim 21 wherein said first inorganic dielectric layer comprises one of the group containing: CORAL, BLACK DIAMOND, FSG, carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, and HSQ.

29. The method according to Claim 26 wherein said second organic dielectric layer comprises one of the group containing: polyimides, HOSP, SILK, FLARE, BCB, MSQ, and organic polymers.

30. The method according to Claim 21 further comprising filling said dual damascene openings with a metal layer.